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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,835	BARROW, MICHAEL	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0804//17 Aug 2004*. → Total of 17 sheets.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present application is a Continuation of application 09/274,430, filed March 22, 1999 (now US Pat. 6,747,362), which is a Continuation of application 08/959,546, filed October 24, 1997 (now US Pat. 5,894,410), which is a Continuation of application 08/623,355, filed March 28, 1996 (abandoned). All prior art made of record in the parent Applications has been considered in the examination of the instant Continuation application.

Specification

2. The disclosure is objected to because of the following informalities:

On p.6, line 8: "16" should be changed to –18–.

On p.6, line 18: "16" should be changed to –18–.

On p.7, line 14: "38" should be changed to –36–.

On p.7, line 17: "38" should be changed to –36–.

On p.7, line 21: "16" should be changed to –18–.

On p.8, line 2: "16" should be changed to –18–.

On p.8, line 3: "20" should be changed to –22–.

On p.8, line 27: "10" should be changed to –10′–.

On p.9, line 5: "60" should be changed to –10′–.

Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

(i) Suyama et al. (US 5,731,630).

(ii) *Electronic Design* (February 6, 1995 issue; article by Jonathan L. Houghten, pp.141-146: *Plastic Ball-Grid Arrays Continue to Evolve*).†

(iii) *Surface Mount International* (Proceedings of Aug.30-Sept.1, 1994; paper by Abbas I. Attarwala et al., pp.252-257: *Failure Mode Analysis of a 540 Pin Plastic Ball Grid Array*).††

(iv) *Surface Mount International* (Proceedings of Aug.29-31, 1995; paper by Freyman et al., pp.373-382: *The Move to Perimeter Plastic BGAs*).†††

†*Already of record in Applicant's IDS, filed August 17, 2004 in the instant Continuing Application (from p.11 of 11 in Form PTO-1449 filed November 07, 2001 in parent Application 09/274,430).*

††*Already of record in Applicant's IDS, filed August 17, 2004 (from p.2 of 11 in Form PTO-1449 filed November 07, 2001 in parent Application 09/274,430).*

†††*Already of record in Applicant's IDS, filed August 17, 2004 (from p.8 of 11 in Form PTO-1449 filed November 07, 2001 in parent Application 09/274,430).*

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 7, 8 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Suyama et al.

A) As to Claim 1, Suyama et al. discloses, in Figs. 1, 2 and 4: a substrate 19 which has a top surface and an opposite bottom surface, the bottom surface having an outer array of contact pads (the bottom surfaces of vias 5) each separated from each other by a first distance, and a center array of contact pads (the bottom surfaces of vias 6) each separated from each other by a second distance (Figs. 1 and 2; col.3: 27-31 and 58-59), the center array of contact pads being separated from the outer array of contact pads by a third distance which is larger than the first and second distances (as defined by the layout shown in Fig. 1); and a plurality of solder balls 10 and 11 attached to the contact pads of substrate 19 (Fig. 2; col.3: 48).

B) As to Claim 2, Suyama et al. further discloses that the top surface of substrate 19 has a plurality of bond pads, the bond pads being the inner ends (leads) 4 of wiring lines 7 that cover (Fig. 2; col.3: 1-5) or cantilever (Fig. 7; col.6: 3-11) substrate openings 3 (Figs. 1 and 4; col.4: 11-17).

C) As to Claim 3, Suyama et al. further discloses that the top surface of substrate 19 has a ground bus 12 that is connected to the center array of contact pads by a plurality of vias 6 that extend through substrate 19 (Figs. 1 and 4; col.3: 30-31 and col.5: 1-8).

D) As to Claim 7, Suyama et al. discloses, in Figs. 1, 2 and 4: a substrate 19 which has a top surface and an opposite bottom surface, the top surface having a plurality of bond pads, the bond pads being the inner ends (leads) 4 of wiring lines 7 that cover (Fig. 2; col.3: 1-5) or cantilever (Fig. 7; col.6: 3-11) substrate openings 3 (Figs. 1 and 4; col.4: 11-17), the bottom surface having an outer array of contact pads (the bottom surfaces of vias 5) each separated from each other by a first distance, and a center array of contact pads (the bottom surfaces of vias 6) each separated from each other by a second distance (Figs. 1 and 2; col.3: 27-31 and 58-59), the center array of contact pads being separated from the outer array of contact pads by a third distance which is larger than the first and second distances (as defined by the layout shown in Fig. 1); a plurality of solder balls 10 and 11 attached to the contact pads of substrate 19 (Fig. 2; col.3: 48); an integrated circuit 8 that is mounted to substrate 19 and coupled to the bond pads (Fig. 4; col.4: 11-17).

E) As to Claim 8, Suyama et al. further discloses that the top surface of substrate 19 has a ground bus 12 that is coupled to integrated circuit 8 and connected to the center array of contact pads by a plurality of vias 6 that extend through substrate 19 (Figs. 1 and 4; col.5: 1-8).

F) As to Claim 13, Suyama et al. further discloses that the outer array of contact pads (the bottom surfaces of vias 5) is located outside an outer dimensional profile of integrated circuit 8 (Figs. 1 and 4).

G) As to Claim 14, Suyama et al. discloses, in Figs. 1, 2 and 4:

a) providing a substrate 19 which has a top surface and an opposite bottom surface, the bottom surface having an outer array of contact pads (the bottom surfaces of vias 5) each separated from each other by a first distance, and a center array of contact pads (the bottom surfaces of vias 6) each separated from each other by a second distance (Figs. 1 and 2; col.3: 27-31 and 58-59), the center array of contact pads being separated from the outer array of contact pads by a third distance which is larger than the first and second distances (as defined by the layout shown in Fig. 1);

b) mounting an integrated circuit 8 to the top surface of substrate 19 (Fig. 4; col.4: 11-17);

c) attaching a plurality of solder balls 10 and 11 (col.3: 48) to the contact pads of substrate 19 (Figs. 2 and 4; col.3: 48).

H) As to Claim 15, Suyama et al. further discloses encapsulating integrated circuit 8 with resin 9 (Fig. 4; col.4: 16).

6. Claims 1, 2, 7 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by *Electronic Design* (article by Jonathan L. Houghten).

A) As to Claim 1, Houghten discloses: a substrate (the 256-lead BGA package on the right side of Fig. 3 on p.144) which has a top surface (best seen in Fig. 1 on p.141) and an opposite bottom surface (Fig. 3 on p.144), the bottom surface having an outer array of contact pads each separated from each other by a first distance (Fig. 3 on p.144; and p.142, the paragraph bridging columns 1 and 2), and a center array of contact pads each separated from each other by a second distance (Fig. 3 on p.144;

and p.142, the full paragraph in the second column), the center array of contact pads being separated from the outer array of contact pads by a third distance which is larger than the first and second distances (Fig. 3 on p.144); and a plurality of solder balls attached to the contact pads of the substrate (Figs. 1 and 3 on pp.141 and 144, respectively; both of the above-cited paragraphs in columns 1 and 2 on p.142).

B) As to Claim 2, Houghten further discloses that the top surface of the substrate has a plurality of bond pads (i.e., the substrate pads that receive the bonding wires; see Fig. 1 on p.141).

C) As to Claim 7, Houghten discloses: a substrate (the 256-lead BGA package on the right side of Fig. 3 on p.144) which has a top surface (best seen in Fig. 1 on p.141) and an opposite bottom surface (Fig. 3 on p.144), the top surface having a plurality of bond pads (i.e., the substrate pads that receive the bonding wires; see Fig. 1 on p.141), the bottom surface having an outer array of contact pads each separated from each other by a first distance (Fig. 3 on p.144; and p.142, the paragraph bridging columns 1 and 2), and a center array of contact pads each separated from each other by a second distance (Fig. 3 on p.144; and p.142, the full paragraph in the second column), the center array of contact pads being separated from the outer array of contact pads by a third distance which is larger than the first and second distances (Fig. 3 on p.144); a plurality of solder balls attached to the contact pads of the substrate (Figs. 1 and 3 on pp.141 and 144, respectively; both of the above-cited paragraphs in columns 1 and 2 on p.142); and an integrated circuit that is mounted to the substrate and coupled to the bond pads (Fig. 1 on p.141).

D) As to Claim 13, Houghten further discloses that the outer array of contact pads is located outside an outer dimensional profile of the integrated circuit (compare Figs. 1 and 3 on pp.141 and 144, respectively).

E) As to Claim 14, Houghten discloses:

a) providing a substrate (the 256-lead BGA package on the right side of Fig. 3 on p.144) which has a top surface (best seen in Fig. 1 on p.141) and an opposite bottom surface (Fig. 3 on p.144), the bottom surface having an outer array of contact pads each separated from each other by a first distance (Fig. 3 on p.144; and p.142, the paragraph bridging columns 1 and 2), and a center array of contact pads each separated from each other by a second distance (Fig. 3 on p.144; and p.142, the full paragraph in the second column), the center array of contact pads being separated from the outer array of contact pads by a third distance which is larger than the first and second distances (Fig. 3 on p.144); and a plurality of solder balls attached to the contact pads of the substrate (Figs. 1 and 3 on pp.141 and 144, respectively; both of the above-cited paragraphs in columns 1 and 2 on p.142);

b) mounting an integrated circuit to the top surface of the substrate (Fig. 1 on p.141);

c) attaching a plurality of solder balls to the contact pads (Figs. 1 and 3 on pp.141 and 144, respectively; both of the above-cited paragraphs in columns 1 and 2 on p.142).

F) As to Claim 15, Houghten further discloses encapsulating the integrated circuit (Fig. 1 on p.141).

G) As to Claim 16, Houghten further discloses coupling the integrated circuit to the substrate with a plurality of bond wires (Fig. 1 on p.141).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

8. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Electronic Design (article by Jonathan L. Houghten).

As to Claims 3 and 8:

I. Houghten further discloses a plurality of ground/thermal vias that extend from the top surface through the 256-lead BGA substrate to the center array contact pads on the bottom surface and the ground/thermal bumps thereon (Fig. 3 on p.144 and the full paragraph in the second column of p.142) but is silent as to whether or not there is a ground bus on the top surface of the substrate.

II. Houghten further teaches an embodiment of a BGA package having ground, as well as power, busses (i.e., ground and power rings) and an integrated circuit mounted on a top surface thereof, wherein the power and ground busses are coupled to the integrated circuit by bonding wires, and connected by a plurality of vias that extend

through the substrate to the center array of contact pads--i.e. masked metal islands--in order to reduce the parasitic inductances in the power and ground connections to and from the integrated circuit, thus ensuring reliable electronic package performance (Fig. 5 on p.146 and the full paragraph in the first column and the paragraph bridging the first and second columns of p.144).

III. Since both the embodiments of Figs. 3 and 5 are BGA integrated circuit packages, then the problem of parasitic inductances on ground, as well as power, connections to and from the integrated circuit would have been readily recognized in the package of Fig. 3 as well as the package of Fig. 5, and the solution of the problem in package of Fig. 5 would have been readily recognized for solving the same problem in the package of Fig. 3.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the BGA package of Fig. 3 with ground AND power busses on the top surface thereof that are coupled to the integrated circuit and connected to the center array of contact pads by a plurality of vias that extend through the substrate, as taught in the package embodiment of Fig. 5, in order to reduce the line length of the ground AND power wiring, thus reducing the parasitic inductances on the ground and power lines and thereby further enhancing the reliability of the BGA package of Fig. 3, as taught in the embodiment in Fig. 5.

9. Claims 4, 5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houghten, as applied to Claims 3 and 8, above, and further in view of *Surface*

Mount International (Proceedings of Aug.30-Sept.1, 1994; paper by Abbas I. Attarwala et al.).

A) As to Claims 4 and 9:

I. Houghten discloses, in Fig. 3, a 256 BGA package with a four row outer array of contact pads and further teaches the use of a ground/thermal central array of contacts (p.142: full paragraph in the first column, the paragraph bridging the first and second columns and the full paragraph of the second column). Houghten also contemplates even larger BGA packages (p.142, in the paragraph bridging the first and second columns) but does not teach that the larger arrays may require outer arrays with more than four rows of contact pads; i.e., specifically, an outer array having at least five rows of contact pads.

II. Attarwala et al. discloses one such BGA with 540 outer array contact pads arranged in a five row pattern in order to compactly accommodate the larger outer array of contact pads (Fig. 2 on p. 253).

III. Since both Houghten and Attarwala et al. teach the fabrication of BGA packages with perimeter (outer) arrays of contact pads, then the five row arrangement of the outer array of contact pads for accommodating the larger 540 pad BGA taught in Attarwala et al. would have been readily recognized as a compact outer array configuration for accommodating the larger perimeter arrays contemplated in the pertinent art of Houghten.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the perimeter BGA packages having a larger

number of contact pads, as contemplated in Houghten, with outer arrays of contact pads having five or more rows in the perimeter arrangement in order to accommodate the larger number of contact pads, as taught by Attarwala et al.

B) As to Claims 5 and 10:

I. Modified Houghten teaches that the top surface of the substrate has a ground bus that is connected to the center array of contact pads by a plurality of vias that extend through the substrate, as discussed in Claim 3, from which Claim 5 indirectly depends, but does not teach that the top surface of the substrate in Fig. 3 has a power bus that is connected to the center array of contact pads by a plurality of vias that extend through the substrate.

II. Modified Houghten further teaches, in Fig. 5, an embodiment of BGA package having both power and ground busses (i.e., power and ground rings) on a top surface thereof, wherein the power and ground busses are connected by a plurality of vias that extend through the substrate to a center array of contact pads--i.e. masked metal islands--in order to reduce the parasitic inductances in the power and ground connections to and from the integrated circuit, thus ensuring reliable electronic package performance (Fig. 5; p.144, the full paragraph in the first column and the paragraph bridging the first and second columns).

III. Since both the embodiments of Figs. 3 and 5, in Houghten, are BGA integrated circuit packages, then the problem of parasitic inductances on power, as well as ground, connections to and from the integrated circuit would have been readily recognized in the package of Fig. 3 as well as the package of Fig. 5, and the solution of

the problem in the package of Fig. 5 would have been readily recognized for solving the same problem in the package of Fig. 3.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the BGA package of Fig. 3 with ground AND power busses on the top surface thereof that are connected to the center array of contact pads by a plurality of vias that extend through the substrate, as taught in the package embodiment of Fig. 5, in order to reduce the line length of the ground AND power wiring, thus reducing the parasitic inductances on the ground and power lines and thereby further enhancing the reliability of the BGA package of Fig. 3, as taught in the embodiment in Fig. 5.

10. Claims 6, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houghten and Attarwala et al., as applied to Claims 5 and 10, above, and further in view of *Surface Mount International* (Proceedings of August 29-31, 1995; paper by Bruce Freyman et al.).

A) As to Claims 6 and 11:

I. Modified Houghten discloses a small matrix of solder balls in the center for applications requiring thermal dissipation, ground and power connections to and from the integrated circuit chip mounted on the top surface and a PCB board on which the package is mounted but does not disclose a specific arrangement; e.g., a four by four matrix (p.142, full paragraph in the second column).

II. Freyman et al. discloses BGA perimeter packages of various sizes and pin counts having a center array matrix with a pin count and dimension suitable for the size

and application of the BGA package (compare the 6 x 6 central array matrix of the 388 pin perimeter BGA in Fig. 1, p.374, with the 3 x 3 central array matrix of the smaller 208 pin perimeter BGA in Fig. 3, p.375).

III. Since both modified Houghten and Freyman et al. disclose BGA packages of various sizes and pin counts, then adjusting the matrix dimensions of the center array of contact pads in a BGA package to the physical size and electronic application of the package, as taught in Freyman et al., would have been readily recognized in the BGA packaging art of Houghten.

IV. Therefore, it would have been an obvious matter of engineering choice, bounded by well-known manufacturing and applications constraints, and ascertainable by routine experimentation and optimization to choose a 4 x 4 matrix of center array pads for the reasons discussed above, and furthermore because the Applicant has not disclosed that, in view of the applied prior art of modified Houghten and Freyman et al., the limitation of the center array of contact pads in an arrangement of, specifically, a 4 x 4 matrix is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical to the function of the claimed BGA package.

B) As to Claim 12, modified Houghten discloses that the integrated circuit is enclosed by an encapsulant (Fig. 1 on p.141).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chu et al. (US 5,686,699) [Already of record in Applicant's IDS, filed August 17, 2004 in the instant Continuing Application *(from p.1 of 11 in Form PTO-1449 filed November 07, 2001 in parent Application 09/274,430)*] and Chu et al. (US 5,703,402) disclose a BGA perimeter array with center and outer contact pad arrays, wherein the outer contact pad arrays have five rows of contact pads. See Fig. 4 in US 5,686,699 and Figs. 2 and 3 in US 5,703,402.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
November 08, 2004